CLAIMS:

1. A method of detecting the ground offset of parts of a network system, more particularly of testing the ground contact between network control units, where data are sent and received over at least one bus system, characterized in

[a] that in the idle state of at least one bus line (10, 12) provided for receiving data and/or of at least one receiver line (24), after a predefinable first time period has elapsed, the level voltage (14) of this at least one bus line (10, 12) is scanned and compared with at least one predefinable limit or reference potential value (80),

[b] that if the limit or reference potential value (80) is exceeded, at least one ground error signal (82) is generated, and

[c] that in dependence on the fact whether until a predefinable second time period has elapsed, which is started at the same time as the predefinable first time period and is longer than the predefinable first time period,

[c.1] the idle state of the at least one bus line (10, 12) or of the at least one receiver line (24) is still there, or

[c.2] the idle state of the at least one bus line (10, 12) or of the at least one receiver line (24) is no longer there, the ground error signal is acknowledged or not acknowledged, respectively.

2. A method as claimed in claim 1, characterized in that in the space of time between the end of the predefinable first time period and the end of the predefinable second time period the ground error signal (82) generated in the method step [b] is buffered without being output.

3. A method as claimed in claim 2, characterized

- in that in case of the method step [c.1] the ground error signal (82) is output after the predefinable second time period has elapsed, or
- in that in case of the method step [c.2] a ground error signal (82) is deleted or reset after the predefinable second time period has elapsed.

4. A method as claimed in at least one of the claims 1 to 3, characterized in that the predefinable first time period and the predefinable second time period are adapted to the bit rate of the bus line (10, 12).

5. A circuit arrangement (100) for detecting the ground offset of parts of a network system, more particularly for checking ground contact between network control units while data can be sent and received over at least one bus system, characterized by

- at least one comparator unit (70) which is assigned to at least one bus line (10, 12) provided for the received data and leading to at least one receiver unit (20), while in the idle state of this at least one bus line (10, 12) and/or at least one receiver line (24) connected downstream of the receiver unit (20), after a first time period has elapsed that can be predefined by at least a first timer unit (30), the level voltage (14) of this at least one bus line (10, 12) can be scanned and compared to at least one predefinable limit or reference potential value (80) by means of the comparator unit (70),
- at least a first switch or trigger element (40) connected downstream of the first timer unit (30) for buffering at least one ground error signal (82) produced by the comparator unit (70) when the limit or reference potential value (80) is exceeded,
- at least a second switch or trigger element (60) connected downstream of at least a second timer unit (50) for taking over or transferring the ground error signal (82) for the case where the idle state of the at least one bus line (10, 12) or of the at least one receiver line (24) still exists until a second time period that can be predefined by the second timer unit (50) has elapsed, which second time period is started at the same time as the predefinable first time period and lasts longer than the predefinable first time period.

6. A circuit arrangement as claimed in claim 5, characterized

- in that the bus system (10, 12) is arranged as a Controller Area Network (CAN) bus systemhaving at least one CANH[igh] bus line (10) and
at least one CANL[ow] bus line (12), and
- in that the output terminal (22) of the receiver unit (20)
is connected both to the input terminal (32) of the first timer unit (30)
nd to the input terminal (52) of the second timer unit (50),
- in that the first switch or trigger element (40) is arranged as a first flipflop element, more particularly as a first D[elay] flipflop element and

- in that the second switch or trigger element (60) is arranged as a second flipflop element more particularly as a second D[elay] flipflop element.

7. A circuit arrangement as claimed in claim 5 or 6, characterized
- in that the output terminal (34) of the first timer unit (30) is connected to the clock input (42) of the first D[elay] flipflop element (40),
- in that the output terminal (76) of the comparator unit (70) is connected to the D-input (44) of the first D[elay] flipflop element (40),
- in that the output terminal (54) of the second timer unit (50) is connected to the clock input (62) of the second D[elay] flipflop element (60) and
- in that the Q-output (46) of the first D[elay] flipflop element (40) is connected to the D-input (64) of the second D[elay] flipflop element (60).

8. A circuit arrangement as claimed in at least one of the claims 5 to 7, characterized in that the second timer unit (50) is connected in parallel to the first timer unit (30).

9. A circuit arrangement as claimed in at least one of the claims 5 to 8, characterized in that
- the delay of the first timer unit (30) and
- the delay of the second timer unit (50) can be adapted to the bit rate of the bus line (10, 12).

10. A use of a method as claimed in at least one of the claims 1 to 4 and/or at least a circuit arrangement (100) as claimed in at least one of the claims 5 to 9 for detecting the ground offset of parts of a network system, more particularly for checking the ground contact between network control units in automotive electronics, more particularly in the electronics of motor vehicles.